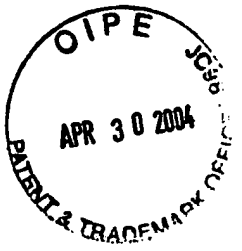

BOX ISSUE FEE
PATENT
2557-000043/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	Kyu-Nam LIM	CONF. NO.: 5338
SERIAL NO.:	09/971,991	GROUP: 2816
FILED:	October 4, 2001	EXAMINER: Linh M. Nguyen
FOR:	INPUT BUFFER CIRCUIT SUPPORTING A LOW VOLTAGE INTERFACE AND A GENERAL LOW VOLTAGE TRANSISTOR LOGIC (LVVTL) INTERFACE	

MAIL STOP BOX ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 30, 2004

COMMENTS ON THE EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Sir:

In reply to the Examiner's Statement of Reasons for Allowance, provided with the Notice of Allowance dated February 3, 2004, Applicants submit the following comments.

The Examiner offers several reasons why the claims of the present application are allowable over the prior art of record. Although Applicants agree that the various claimed limitations mentioned in the claims are not taught or suggested by the prior art taken either singly or in combination, Applicants wish to emphasize that it is each claim, taken as a whole, including the interrelationships and interconnections between various claimed elements which is allowable over the prior art of record.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano, Reg. No. 35,094 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

John A. Castellano, Reg. No. 35,094
P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/cah